CLAIMS:

Please amend claims 1, 6, 17, 19 and 20. Please cancel claim 18. Please add new claim 21. Claims are as follows:

1. (Currently Amended) A method of detecting an interconnection structure having a region within a first wiring level wherein a second layer is not covering a first layer, comprising:

providing the first layer having the second layer on a surface of the first layer; ~~and~~

forming an at least one conductive feature within the first and second layers; and

performing a process to clean an exposed surface of the conductive feature, wherein the process forms ~~creating~~ a recess in the first layer in the region where the second layer is not covering the first layer.

2. (Original) The method of claim 1, wherein the recess is created by selectively etching the first layer in the region where the second layer is not covering the first layer.

3. (Original) The method of claim 2, wherein at least one of a group of conditions of the selective etch are altered to change a depth of the recess, wherein the group of conditions is selected from a group consisting of: etching material, temperature, power, pressure, and duration of the process.

4. (Original) The method of claim 2, wherein the selective etch is performed by a reducing plasma preclean process.

5. (Original) The method of claim 4, wherein the reducing plasma preclean process uses a plasma selected from the group consisting of: H_2, N_2, NH_3 and noble gases.

6. (Currently Amended) The method of claim 1, wherein the first layer comprises a dielectric material ~~selected from a group consisting of: a SiLK™ semiconductor dielectric resin, Teflon, bezocyclobutane BCB, parylene N, parylene F, SiCOH, porous SiO_2, silica aerogels, and Flare™~~.

7. (Original) The method of claim 1, wherein the second layer comprises a hardmask selected from a group consisting of: SiN_x, SiO_xN_y, SiC_x, SiO_xC_y, SiC_xN_y, SiO_2, and $SiC_xO_yH_z$.

8. (Original) The method of claim 1, wherein the first layer comprises a material that etches selectively to the second layer with a selectivity of greater than 1 to 1.

9. (Original) The method of claim 1, after creating a recess in the first layer, further comprising: forming a plurality of conductive features within a second wiring level of the structure.

10. (Original) The method of claim 9, wherein the conductive features comprise:

a liner comprising a material selected from the group consisting of: tantalum-based materials, tungsten-based materials and titanium-based materials; and

a conductive material selected from the group consisting of: copper, gold, platinum and

silver.

11. (Original) The method of claim 9, wherein an electrical short between conductive features results if the recess in the first wiring level replicates in the second wiring level, wherein conductive features are selected from a group consisting of: wires, vias, and wires and vias.

12. (Original) The method of claim 11, further comprising:

rejecting the interconnection structure if the recess replicates in the second wiring level.

13. (Withdrawn) A structure comprising:

a first wiring level of the structure comprising:

a first layer covering a surface of the structure;

a second layer substantially covering a surface of the first layer; and

a recess formed in a region of the structure where the second layer does not cover the first layer; and

a second wiring level of the structure comprising:

a third layer having a replicated recess in the third layer in the region of the structure where the second layer does not cover the first layer.

14. (Withdrawn) The structure of claim 13, wherein the first layer comprises a dielectric material selected from a group consisting of: a SiLK™ semiconductor dielectric resin, Teflon, bezocyclobutane-BCB, parylene-N, parylene-F, SiCOH, porous SiO_2, silica aerogels, and

Flare™.

15. (Withdrawn) The structure of claim 13, wherein the second layer comprises a hardmask selected from a group consisting of: SiN_x, SiO_xN_y, SiC_x, SiO_xC_y, SiC_xN_y, SiO_2, and $SiC_xO_yH_z$.

16. (Withdrawn) The structure of claim 13, wherein the replicated recess in the third layer in the region of the structure where the second layer does not cover the first layer produces an electrical short between conductive features within the third layer, wherein the conductive features are selected from a group consisting of: wires, vias, and wires and vias.

17. (Currently Amended) A method of forming an interconnection structure, comprising:

forming a first wiring level comprising a first layer, a second layer on a surface of the first layer, and at least one conductive feature within the first and second layers;

performing a preclean process on a surface of the first wiring level, wherein the preclean process forms a recess within the first layer in a region of the first wiring level where the second layer does not cover the first layer; and

forming a second wiring level on a surface of the first wiring level comprising a third layer on the surface of the first wiring level and a plurality of conductive features within the third layer, wherein the recess within the first layer of the first wiring level is replicated in the third layer of the second wiring level producing an electrical short between at least two of the plurality of conductive features within the second wiring level.

~~using recessed topography formed within a first layer of the structure to indicate the~~

~~absence of a hardmask covering the first layer.~~

18. (Canceled) The method of claim 17, wherein using the recessed topography within the first layer comprises:

etching the first layer of the structure in a region where the hardmask is not covering the first layer; and

leaving the first layer unetched in a region where the hardmask covers the first layer.

19. (Currently Amended) The method of claim ~~18~~ 17, wherein ~~etching the first layer of the structure~~ performing the preclean process on the surface of the first wiring level employs a reducing plasma preclean process.

20. (Currently Amended) The method of claim 19, wherein the reducing plasma preclean process etches the first layer selectively to the ~~hardmask~~ second layer.

21. (New) The method of claim 19, wherein at least one of a group of conditions of the reducing plasma preclean process are altered to change a depth of the recess within the first layer, wherein the group of conditions is selected from a group consisting of: etching material, temperature, power, pressure, and duration of the process.